A New Method Of Digital FM Demodulator

BACKGROUND OF THE INVENTION

1.Field of the invention

The present invention relates to a new method of digital frequency-modulation demodulator , and more particularly, to a digital frequency-modulation demodulator that using the structure of time-to-digital converter and the concept of delta-sigma analog-to-digital converter .

2.Description Of The Prior Art

The frequency modulation (FM) is one of important and common method in radio communication system that its receiver end contains the FM demodulation circuit which often using analog design circuit and the conventional analog style FM demodulation circuit including detector circuit and phase lock loop circuit . If bring the detector into integrated circuit then it need bigger chip area, and if implement PLL into integrated circuit then an external capacitor is necessary outside this chip .

If the modulated signal need the digital signal process after demodulation , then the above two circuit need analog-to-digital converter to convert the demodulated analog signal into digital signal , meanwhile, this analog signal is easy to be interfered by noise signal . However, the digital FM demodulator will first convert the modulation intermediate-frequency (IF) signal into digital signal by way of analog-to-digital converter, then using digital signal processor to demodulate this modulation signal . The analog-to-digital converter and digital signal processor used in digital FM demodulator must have fast speed to demodulate the modulation signal in real time . It also could use reference clock with multiple-fold frequency of modulation signal for sampling the input modulation signal to detect its phase change then demodulate, but such technology need a high frequency reference clock .

The conventional methods of digital RF communication system always need to convert the analog signal into digital signal in the receiver end with drawbacks that increasing the circuit complexity . Thus, the demodulation circuit combines the detector circuit or PLL with analog-to-digital circuit could simply the circuit design also will be one of major objectives today .

SUMMARY OF THE INVENTION

It is therefore a primary objective of the present invention to provide a new method of digital FM demodulator will be applicable in radio communication system, besides, the modulation-demodulation section in receiver end also could be applicable in BB call , cellular phone , GPS system , and DECT system .

The next objective of the present invention is to provide a digital FM demodulator with two function of modulation-demodulation and analog-to-digital conversion ◦ The input intermediate-frequency signal pass through this invention demodulator will generate a digital signal including high-frequency quantized signal ， then by way of a low-pass filter to filter out above quantized noise signal to get the basedband signal ◦

The other objective of the present invention is to provide a digital FM demodulator which adopt the PLL structure and utilize the concept of delta-sigma analog-to-digital converter which without connect external component and high frequency reference clock so that easy for integration ◦

This invention with advantages that not only use delay lines as the timing reference but also adopt the concept of delta-sigma analog-to-digital converter to achieve the time-to-digital conversion for digital FM demodulator ◦ This digital FM demodulator including delay lines ， m-to-1 multiplexer ， phase detector ， charge pump circuit ， quantizer and digital integrator ◦ The modulation signal in intermediate frequency segment pass through the delay lines with the delay time around one cycle time ， and this delayed signal compare its phase with original signal ◦ This compared pulse will go through charge pump circuit and convert into a voltage level stored in capacitor ◦ This quantized voltage is accumulated by the digital integrator, then sample another output signal of delay lines and compare phase with input signal ◦ This system is similar to PLL , is a feedback system ◦ The quantized digital signal will feed through low-pass filter to filter out high frequency noise and get the original modulation signal, this modulation signal is a digital signal ◦

BRIEF DESCRIPTION OF THE DRAWINGS

The drawings disclose an illustrative embodiment of the present invention Which serves to exemplify the various advantages and objects hereof, and are as follows:

Fig.1 is the circuit block diagram of digital FM demodulator according to the present invention ◦

Fig.2 is the circuit waveform of digital FM demodulator according to the present invention ◦

Fig.3 is the system structure of digital FM demodulator according to the present invention ◦

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Please refer to Fig.1 that relates to the circuit block diagram of digital FM demodulator ◦ The modulation signal Ai(t) is fed into reference delay lines 11 ， said reference delay lines-11 including coarse delay line 111 and fine delay line 112 ， those delay time of delay lines 111 and 112 is controlled separately by other circuits ◦ The fine delay lines 112 has multiple output signal Ai1(t),Ai2(t),Ai3(t)..... Aij(t) which could be expressed as follow:

$Aij(t)=Ai(t-Tc-j*\tau)$ ----- (1)

Tc: the total fixed delay time of coarse delay lines

τ : the unit delay time of fine delay lines

The phase detector compares the phase difference between Aid and Ai,then generate up and down signal.The m-to-1 multiplexer will select one of output signal Ai0(t), Ai1(t),Ai2(t) ---- Aij(t) from fine delay lines 112 and name it as Aid signal ◦ If the rising edge of Aid signal lead the Ai signal ， up signal will generate an effective pulse and its pulse width is just same as the time difference between the rising edges of Ai and Aid, but down signal do not genarate any effective pulse ◦ The total delay time of Ai signal pass through delay lines is "$Tc+d*\tau$ ", and the pulse width will equal to "$T-Tc-d*\tau$ " when "$Tc+d*\tau$ " smaller than period T of Ai signal ◦

In the same way ， if the rising edge of Aid signal lag the Ai signal ， down signal will generate an effective pulse and its pulse width is also just same as the time difference of Aid and Ai signal, and the pulse width will equal to "$Tc+d*\tau-T$" ◦

Its value is positive when Aid lead the Ai signal, on the contrary, its value is negative when Aid lag Ai signal ◦ Both effective pulse of up and down signal will trigger the charge pump circuit 14 for charging and discharging to capacitor Cc which will generate a voltage difference ΔVf ， and its voltage level is proportional to the time difference or phase difference of Aid and Ai signal ◦

Each cycle of input modulated signal will generate a ΔVf which is accumulated in stored capacitor Cc and this stored voltage will be quantized to generate a bit stream digital signal y(k), y(k) is the output digital sequence of total system ◦

Quantizer 15 is a analog-to-digital converter which could be one bit or multiple bit converter ◦ One bit converter is the comparator ， The quantizer 15 in this invention adopt one bit voltage comparator ◦

Digital integrator 16 accumulate output digital signal y(k), actually, it is simply an up-down counter due to quantizer 15 is one bit analog-digital converter ◦ The counter output signal will select one output Aid signal from the fine delay lines by way of multiplexer and compare its phase with Ai

signal。Consequently，the delay time of Aid signal is controlled by output signal y(k)，it will delay one more unit time if y(k)=1，On the contrary，the delay of Aid decrease one unit delay if y(k)=0。Thus，this whole system is similar to PLL structure，Y(K) is feedback to adjust the Aid delay time and make the next rising edge of Ai signal arrive phase detector with rising edge of Aid signal simultaneously，so the Aid signal is just delayed one cycle than Ai signal when the system is locked。

As shown in Fig.2，this is the circuit waveform of digital FM demodulator according to the present invention。T(k) is the kth cycle time of input modulation signal and P(k) is the time difference of Aid rising edge with next Ai cycle。The effective pulse of up signal means P(k) is positive value，but the down signal make P(K) negative。That is because the maximum frequency shift of input modulation signal is much smaller than carrier frequency。The change of T(k) is small relative to carrier cycle Tc。

Therefore，the effective pulse of up signal and down signal only happen at rising edge of Aid and Ai signal，and this effective pulse has been transferred to ΔVf that is stored in capacitor Cc by way of charge pump circuit before arriving of falling edge。This falling edge could be the trigger clock of the quantizer and counter，

That means this system do not need external reference clock。As shown in Fig.2 waveform diagram，a formula as follows：

$$P(k+1)=P(k)+T(k)-T(k-1)+y(k)*\tau \quad \text{------ (2)}$$

Definition:

$$\Delta T(k)=T(k)-T(k-1) \quad \text{------ (3)}$$

Therefore, we could get;

$$P(k+1)=P(k)+\Delta T(k)+y(k)*\tau \quad \text{------ (4)}$$

If V(k) means the capacitor voltage at kth cycle，based on Fig.2, we could see V(k) signal is generated by V(k-1) and Ic signal to charge/discharge Cc during up or down signal effective pulse period and Ib charge/discharge Cc during kth cycle，i.e. the voltage is determined by these three parameters。

The voltage on Cc for Ic at kth cycle is：

$$\Delta Vf\_a=Ic/Cc*P(k) \quad \text{------ (5)}$$

If the trigger clock is the input modulation signal Ai，then the Cc voltage level will be next formula when charge-discharge is at kth cycle。

$$\Delta Vf\_b=y(k)*Ib/Cc*[T(k)+T(k+1)]/2 \quad \text{------ (6)}$$

Then

$$\Delta Vf=\Delta Vf\_a+\Delta Vf\_b \quad \text{------ (7)}$$

$$V(k+1)=V(k)+\{y(k)*(Ib/Cc)*[T(k)+T(k+1)]/2\}+\{Ic/Cc*P(k)\} \quad \text{------(8)}$$

Because the maximum frequency shift is much smaller than carrier frequency , the T(k) is around equal to carrier cycle Tc .

$V(k+1)=V(k)+Ic/Cc*P(k)+y(k)*(Ib/Cc)*Tc$ ------ (9)
Assume
$A=Ic/Cc$;
$B=(Ib/Cc)*Tc$
We could get next formula :
$V(k+1)=V(k)+A*P(k+1)+B*y(k)$
Put the P(k+1) into above formula, then get

$V(k+1)=V(k)+A*[P(k)+\Delta T(k)+y(k)*\tau]+B*y(k)$

The quantized output of V(k) is the total system output .

As shown in Fig.3 , is the system structure of digital FM demodulator according to the present invention . This diagram is a two level delta-sigma structure , its input is $\Delta T(k)$ that also is the signal difference of T(k) and T(k-1) .

The concept of the output signal y(k) in present invention is similar to conventional analog-digital converter output signal , the quantized noise signal is shifted to high frequency segment . So , the output digital signal y(k) is accumulated first then filter out quantized noise by the digital filter to get the modulation signal .

These technology is similar to conventional delta-sigma analog-to-digital converter . Based on above deduction , the output digital signal is the differentiation of original modulation signal . In brief , y(k) signal filter out the quantized noise by way of low-pass digital filter before signal accumulation .

This invention provide a FM digital demodulator which with more advantages than conventional technology as follow:

1. the method and circuit in present invention will be applicable in radio communication system, besides, the modulation-demodulation section in receiver end also could be applicable in BB call , cellular phone , GPS system , and DECT system .

2. the present invention to provide a digital modulation demodulator which adopt the PLL structure and utilize the concept of delta-sigma analog-to-digital converter which without connect external component and high frequency reference clock so that easy for integration .